

pg 4



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,558	05/01/2001	Jayakumar Krishnankutty	CISCO-3678	5971

7590 06/04/2004
Timothy A. Brisson
Sierra Patent Group
P.O. Box 6149
Stateline, NV 89449

EXAMINER

LEFKOWITZ, SUMATI

ART UNIT	PAPER NUMBER
----------	--------------

2112

DATE MAILED: 06/04/2004

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/847,558

Applicant(s)

KRISHNANKUTTY, JAYAKUMAR

Examiner

Sumati Lefkowitz

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-7 are pending.

Drawings

2. The drawings are objected to because

- in Figure 3A, elements 308 and 310 have been labeled "Pulse Generating Logic", but should be labeled "Pulse Receiving Logic" to be consistent with the specification

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al., 6,442,446 (hereinafter Nakamura) in view of Farmwald et al., 5,179,670 (hereinafter Farmwald) and further in view of what was well known in the art, as exemplified by any one of Appleby-Allis et al., 2003/0033514 (hereinafter Appleby-Allis), Lerche et al.,

Art Unit: 2112

6,283,227 (hereinafter Lerche), Adler et al., 6,009,409 (hereinafter Adler), and Mendel, 5,986,465.

As to claims 1-3 and 7, Nakamura discloses a system for automatically updating the revision level of programmable devices comprising a master programmable device (i.e., EC 12) having a memory (i.e., version information file 16) space operatively disposed therein, and at least one slave programmable device (i.e., machine controllers MC, 11), the slave programmable device coupled to the master programmable device through an interface (note Figures 2-5) and configured to send revision information to the master programmable device, wherein the memory space further includes a revision register (i.e., version information file 16) containing one or more memory locations, each memory location corresponding to a slave programmable device (note abstract, Figures 2-5, column 1, lines 25-38, column 2, lines 17-28, column 3, line 66 – column 4, line 3, column 4, lines 14-25, column 4, lines 36-51, column 5, line 55 – column 6, line 24, and claim 13).

Nakamura fails to disclose that the master programmable device has pulse receiving logic and the slave programmable device has pulse generating logic, or that the revision information comprises a pulse stream corresponding to the revision level of a slave programmable device, or that the master programmable device is one of a group consisting of an FPGA and an EPLD, or that the slave programmable device is one of a group consisting of an FPGA and an EPLD, or that the slave programmable device is sends revision information to the master programmable device in response to receiving a reset signal.

Farmwald discloses pulse receiving and pulse generating logic for receiving and transmitting pulses, respectively, to identify the slot position of each unit on a bus and the total

Art Unit: 2112

number of units on the bus, so that the information comprises pulse streams corresponding to the number of units and the respective slot positions of the units (note abstract, column 1, line 53 – column 2, line 43 and column 4, line 44 – column 6, line 40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of pulse generating and receiving logic to indicate using a pulse stream device specific information about devices on a bus, as Farmwald teaches, in the system of Nakamura so as to reduce the number of signal lines required to provide device specific information to other devices in the system, as Farmwald teaches at column 1, lines 24-58.

Examiner takes Official Notice that using FPGAs and EPLDs to implement controllers and other means for controlling peripherals and processing data is well known in the art of programmable logic devices, evidence of which may be found in Appleby-Allis at [0093], Lerche at column 3, lines 21-39, Adler at column 5, lines 26-52, or Mendel at column 3, line 48 – column 4, line 2.

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of FPGAs or EPLDs to implement the control functions of the controllers of Nakamura so as to create CPU-like flexibility using only reconfigurable logic and a software design methodology, as Appleby-Allis teaches at [0093], implicitly decreasing the cost required to implement the controllers.

Farmwald discloses that the slave devices send revision information to the master device in response to a user's command (note column 4, lines 38-47 and column 5, lines 19-23). One of ordinary skill in the art would recognize that the actual type of trigger for causing the slaves to send revision information to the master, whether it be a reset signal or a user command, does not

Art Unit: 2112

change the underlying concept of using a trigger to initiate sending revision info from the slaves to the master. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of any type of trigger, including a reset signal, to cause the slaves to send revision info to the master so as to allow for the automatic updating of revision information in the master.

5. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al., 6,442,446 (hereinafter Nakamura) in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As to claims 4 and 5, Nakamura discloses a system for collecting programmable device revision information comprising means for sending, by the at least one slave programmable device (i.e., MC 11), revision information to the master programmable device (i.e., EC 12), means for receiving (i.e., version information collection section 15), by the master programmable device, the revision information, and means for storing (i.e., version information file 16), by the master programmable device, the revision information, wherein the means for storing comprises a revision register containing one or more memory locations, each memory location corresponding to a slave programmable device (note abstract, Figures 2-5, column 1, lines 25-38, column 2, lines 17-28, column 3, line 66 – column 4, line 3, column 4, lines 14-25, column 4, lines 36-51, column 5, line 55 – column 6, line 24, and claim 13).

Nakamura fails to disclose means for sending, by the system, a reset signal to a master programmable device and at least one slave programmable device thereby placing all programmable devices in a known good condition.

Art Unit: 2112

AAPA discloses means for sending, by the system, a reset signal to a master programmable device and at least one slave programmable device thereby placing all programmable devices in a known good condition (note page 6, lines 7-10 and page 7, lines 9-12).

It would have been obvious to one of ordinary skill in the art at the time of the invention to place all programmable devices in a known good condition using a reset signal, as AAPA teaches, in the system of Nakamura so as to insure that all devices are in a predetermined state before collecting revision information, thereby minimizing errors during the collection of revision information.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al., 6,442,446 (hereinafter Nakamura) in view of Applicant's Admitted Prior Art (hereinafter AAPA), as applied to claims 4 and 5 above, and further in view of Farmwald et al., 5,179,670 (hereinafter Farmwald).

As to claim 6, Nakamura and AAPA fail to disclose that the revision information comprises a pulse stream corresponding to the revision level of a slave programmable device.

Farmwald discloses that information sent between units on a bus comprise pulse streams corresponding to the number of units and the respective slot positions of the units (note abstract, column 1, line 53 – column 2, line 43 and column 4, line 44 – column 6, line 40).

It would have been obvious to one of ordinary skill in the art at the time of the invention to employ the use of pulse streams to indicate device specific information about devices on a bus, as Farmwald teaches, in the system of Nakamura and AAPA so as to reduce the number of

Art Unit: 2112

signal lines required to provide device specific information to other devices in the system, as Farmwald teaches at column 1, lines 24-58.

Response to Arguments

7. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2112

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sumati Lefkowitz whose telephone number is 703-308-7790.

The examiner can normally be reached on Monday-Friday from 6:00-2:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at 703-305-4815.

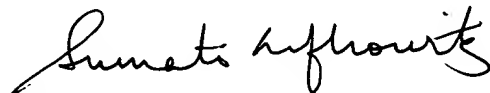
The fax phone numbers for the organization where this application or proceeding is assigned are:

703-746-7238 for After-Final communications

703-872-9306 for Official communications

703-746-5661 for Non-Official/Draft communications

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.



Sumati Lefkowitz
Primary Examiner
Art Unit 2112

sl
May 28, 2004